

APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAME: Dalton et al.

TITLE: FINE-PITCH DEVICE LITHOGRAPHY USING A SACRIFICIAL HARDMASK

DOCKET NO.: FIS9-2001-0168

**INTERNATIONAL BUSINESS MACHINES CORPORATION
NEW ORCHARD ROAD, ARMONK, NY 10504**

CERTIFICATE OF MAILING UNDER 37 CFR 1.10
I HEREBY CERTIFY THAT, ON THE DATE SHOWN BELOW
THIS CORRESPONDENCE IS BEING DEPOSITED WITH
THE UNITED STATES POSTAL SERVICE IN AN ENVELOPE
ADDRESSED TO THE U.S. PATENT AND TRADEMARK
OFFICE, P.O. BOX 2327, ARLINGTON, VA 22202 AS
"EXPRESS MAIL POST OFFICE ADDRESSEE"
MAILING LABEL # _EK602285307US_

On 1/17/02
Karen Cing-Mars
Name of person mailing paper

Signature

Date

10053288-011702

FINE-PITCH DEVICE LITHOGRAPHY USING A SACRIFICIAL HARDMASK

RELATED APPLICATION

5 This application is related to U.S. Application No. 09/550,943 filed April 17, 2000, entitled "Protective hardmask for producing interconnect structures," and assigned to the same assignee as the present application. The disclosure of the related application is incorporated herein by reference.

FIELD OF THE INVENTION

10 This invention relates to semiconductor processing, and more particularly to critical dimension control in deep submicron lithography for fabrication of interconnects in a dual damascene process.

BACKGROUND OF THE INVENTION

15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
90
95
100
105
110
115
120
125
130
135
140
145
150
155
160
165
170
175
180
185
190
195
200
205
210
215
220
225
230
235
240
245
250
255
260
265
270
275
280
285
290
295
300
305
310
315
320
325
330
335
340
345
350
355
360
365
370
375
380
385
390
395
400
405
410
415
420
425
430
435
440
445
450
455
460
465
470
475
480
485
490
495
500
505
510
515
520
525
530
535
540
545
550
555
560
565
570
575
580
585
590
595
600
605
610
615
620
625
630
635
640
645
650
655
660
665
670
675
680
685
690
695
700
705
710
715
720
725
730
735
740
745
750
755
760
765
770
775
780
785
790
795
800
805
810
815
820
825
830
835
840
845
850
855
860
865
870
875
880
885
890
895
900
905
910
915
920
925
930
935
940
945
950
955
960
965
970
975
980
985
990
995
1000
1005
1010
1015
1020
1025
1030
1035
1040
1045
1050
1055
1060
1065
1070
1075
1080
1085
1090
1095
1100
1105
1110
1115
1120
1125
1130
1135
1140
1145
1150
1155
1160
1165
1170
1175
1180
1185
1190
1195
1200
1205
1210
1215
1220
1225
1230
1235
1240
1245
1250
1255
1260
1265
1270
1275
1280
1285
1290
1295
1300
1305
1310
1315
1320
1325
1330
1335
1340
1345
1350
1355
1360
1365
1370
1375
1380
1385
1390
1395
1400
1405
1410
1415
1420
1425
1430
1435
1440
1445
1450
1455
1460
1465
1470
1475
1480
1485
1490
1495
1500
1505
1510
1515
1520
1525
1530
1535
1540
1545
1550
1555
1560
1565
1570
1575
1580
1585
1590
1595
1600
1605
1610
1615
1620
1625
1630
1635
1640
1645
1650
1655
1660
1665
1670
1675
1680
1685
1690
1695
1700
1705
1710
1715
1720
1725
1730
1735
1740
1745
1750
1755
1760
1765
1770
1775
1780
1785
1790
1795
1800
1805
1810
1815
1820
1825
1830
1835
1840
1845
1850
1855
1860
1865
1870
1875
1880
1885
1890
1895
1900
1905
1910
1915
1920
1925
1930
1935
1940
1945
1950
1955
1960
1965
1970
1975
1980
1985
1990
1995
2000
2005
2010
2015
2020
2025
2030
2035
2040
2045
2050
2055
2060
2065
2070
2075
2080
2085
2090
2095
2100
2105
2110
2115
2120
2125
2130
2135
2140
2145
2150
2155
2160
2165
2170
2175
2180
2185
2190
2195
2200
2205
2210
2215
2220
2225
2230
2235
2240
2245
2250
2255
2260
2265
2270
2275
2280
2285
2290
2295
2300
2305
2310
2315
2320
2325
2330
2335
2340
2345
2350
2355
2360
2365
2370
2375
2380
2385
2390
2395
2400
2405
2410
2415
2420
2425
2430
2435
2440
2445
2450
2455
2460
2465
2470
2475
2480
2485
2490
2495
2500
2505
2510
2515
2520
2525
2530
2535
2540
2545
2550
2555
2560
2565
2570
2575
2580
2585
2590
2595
2600
2605
2610
2615
2620
2625
2630
2635
2640
2645
2650
2655
2660
2665
2670
2675
2680
2685
2690
2695
2700
2705
2710
2715
2720
2725
2730
2735
2740
2745
2750
2755
2760
2765
2770
2775
2780
2785
2790
2795
2800
2805
2810
2815
2820
2825
2830
2835
2840
2845
2850
2855
2860
2865
2870
2875
2880
2885
2890
2895
2900
2905
2910
2915
2920
2925
2930
2935
2940
2945
2950
2955
2960
2965
2970
2975
2980
2985
2990
2995
3000
3005
3010
3015
3020
3025
3030
3035
3040
3045
3050
3055
3060
3065
3070
3075
3080
3085
3090
3095
3100
3105
3110
3115
3120
3125
3130
3135
3140
3145
3150
3155
3160
3165
3170
3175
3180
3185
3190
3195
3200
3205
3210
3215
3220
3225
3230
3235
3240
3245
3250
3255
3260
3265
3270
3275
3280
3285
3290
3295
3300
3305
3310
3315
3320
3325
3330
3335
3340
3345
3350
3355
3360
3365
3370
3375
3380
3385
3390
3395
3400
3405
3410
3415
3420
3425
3430
3435
3440
3445
3450
3455
3460
3465
3470
3475
3480
3485
3490
3495
3500
3505
3510
3515
3520
3525
3530
3535
3540
3545
3550
3555
3560
3565
3570
3575
3580
3585
3590
3595
3600
3605
3610
3615
3620
3625
3630
3635
3640
3645
3650
3655
3660
3665
3670
3675
3680
3685
3690
3695
3700
3705
3710
3715
3720
3725
3730
3735
3740
3745
3750
3755
3760
3765
3770
3775
3780
3785
3790
3795
3800
3805
3810
3815
3820
3825
3830
3835
3840
3845
3850
3855
3860
3865
3870
3875
3880
3885
3890
3895
3900
3905
3910
3915
3920
3925
3930
3935
3940
3945
3950
3955
3960
3965
3970
3975
3980
3985
3990
3995
4000
4005
4010
4015
4020
4025
4030
4035
4040
4045
4050
4055
4060
4065
4070
4075
4080
4085
4090
4095
4100
4105
4110
4115
4120
4125
4130
4135
4140
4145
4150
4155
4160
4165
4170
4175
4180
4185
4190
4195
4200
4205
4210
4215
4220
4225
4230
4235
4240
4245
4250
4255
4260
4265
4270
4275
4280
4285
4290
4295
4300
4305
4310
4315
4320
4325
4330
4335
4340
4345
4350
4355
4360
4365
4370
4375
4380
4385
4390
4395
4400
4405
4410
4415
4420
4425
4430
4435
4440
4445
4450
4455
4460
4465
4470
4475
4480
4485
4490
4495
4500
4505
4510
4515
4520
4525
4530
4535
4540
4545
4550
4555
4560
4565
4570
4575
4580
4585
4590
4595
4600
4605
4610
4615
4620
4625
4630
4635
4640
4645
4650
4655
4660
4665
4670
4675
4680
4685
4690
4695
4700
4705
4710
4715
4720
4725
4730
4735
4740
4745
4750
4755
4760
4765
4770
4775
4780
4785
4790
4795
4800
4805
4810
4815
4820
4825
4830
4835
4840
4845
4850
4855
4860
4865
4870
4875
4880
4885
4890
4895
4900
4905
4910
4915
4920
4925
4930
4935
4940
4945
4950
4955
4960
4965
4970
4975
4980
4985
4990
4995
5000
5005
5010
5015
5020
5025
5030
5035
5040
5045
5050
5055
5060
5065
5070
5075
5080
5085
5090
5095
5100
5105
5110
5115
5120
5125
5130
5135
5140
5145
5150
5155
5160
5165
5170
5175
5180
5185
5190
5195
5200
5205
5210
5215
5220
5225
5230
5235
5240
5245
5250
5255
5260
5265
5270
5275
5280
5285
5290
5295
5300
5305
5310
5315
5320
5325
5330
5335
5340
5345
5350
5355
5360
5365
5370
5375
5380
5385
5390
5395
5400
5405
5410
5415
5420
5425
5430
5435
5440
5445
5450
5455
5460
5465
5470
5475
5480
5485
5490
5495
5500
5505
5510
5515
5520
5525
5530
5535
5540
5545
5550
5555
5560
5565
5570
5575
5580
5585
5590
5595
5600
5605
5610
5615
5620
5625
5630
5635
5640
5645
5650
5655
5660
5665
5670
5675
5680
5685
5690
5695
5700
5705
5710
5715
5720
5725
5730
5735
5740
5745
5750
5755
5760
5765
5770
5775
5780
5785
5790
5795
5800
5805
5810
5815
5820
5825
5830
5835
5840
5845
5850
5855
5860
5865
5870
5875
5880
5885
5890
5895
5900
5905
5910
5915
5920
5925
5930
5935
5940
5945
5950
5955
5960
5965
5970
5975
5980
5985
5990
5995
6000
6005
6010
6015
6020
6025
6030
6035
6040
6045
6050
6055
6060
6065
6070
6075
6080
6085
6090
6095
6100
6105
6110
6115
6120
6125
6130
6135
6140
6145
6150
6155
6160
6165
6170
6175
6180
6185
6190
6195
6200
6205
6210
6215
6220
6225
6230
6235
6240
6245
6250
6255
6260
6265
6270
6275
6280
6285
6290
6295
6300
6305
6310
6315
6320
6325
6330
6335
6340
6345
6350
6355
6360
6365
6370
6375
6380
6385
6390
6395
6400
6405
6410
6415
6420
6425
6430
6435
6440
6445
6450
6455
6460
6465
6470
6475
6480
6485
6490
6495
6500
6505
6510
6515
6520
6525
6530
6535
6540
6545
6550
6555
6560
6565
6570
6575
6580
6585
6590
6595
6600
6605
6610
6615
6620
6625
6630
6635
6640
6645
6650
6655
6660
6665
6670
6675
6680
6685
6690
6695
6700
6705
6710
6715
6720
6725
6730
6735
6740
6745
6750
6755
6760
6765
6770
6775
6780
6785
6790
6795
6800
6805
6810
6815
6820
6825
6830
6835
6840
6845
6850
6855
6860
6865
6870
6875
6880
6885
6890
6895
6900
6905
6910
6915
6920
6925
6930
6935
6940
6945
6950
6955
6960
6965
6970
6975
6980
6985
6990
6995
7000
7005
7010
7015
7020
7025
7030
7035
7040
7045
7050
7055
7060
7065
7070
7075
7080
7085
7090
7095
7100
7105
7110
7115
7120
7125
7130
7135
7140
7145
7150
7155
7160
7165
7170
7175
7180
7185
7190
7195
7200
7205
7210
7215
7220
7225
7230
7235
7240
7245
7250
7255
7260
7265
7270
7275
7280
7285
7290
7295
7300
7305
7310
7315
7320
7325
7330
7335
7340
7345
7350
7355
7360
7365
7370
7375
7380
7385
7390
7395
7400
7405
7410
7415
7420
7425
7430
7435
7440
7445
7450
7455
7460
7465
7470
7475
7480
7485
7490
7495
7500
7505
7510
7515
7520
7525
7530
7535
7540
7545
7550
7555
7560
7565
7570
7575
7580
7585
7590
7595
7600
7605
7610
7615
7620
7625
7630
7635
7640
7645
7650
7655
7660
7665
7670
7675
7680
7685
7690
7695
7700
7705
7710
7715
7720
7725
7730
7735
7740
7745
7750
7755
7760
7765
7770
7775
7780
7785
7790
7795
7800
7805
7810
7815
7820
7825
7830
7835
7840
7845
7850
7855
7860
7865
7870
7875
7880
7885
7890
7895
7900
7905
7910
7915
7920
7925
7930
7935
7940
7945
7950
7955
7960
7965
7970
7975
7980
7985
7990
7995
8000
8005
8010
8015
8020
8025
8030
8035
8040
8045
8050
8055
8060
8065
8070
8075
8080
8085
8090
8095
8100
8105
8110
8115
8120
8125
8130
8135
8140
8145
8150
8155
8160
8165
8170
8175
8180
8185
8190
8195
8200
8205
8210
8215
8220
8225
8230
8235
8240
8245
8250
8255
8260
8265
8270
8275
8280
8285
8290
8295
8300
8305
8310
8315
8320
8325
8330
8335
8340
8345
8350
8355
8360
8365
8370
8375
8380
8385
8390
8395
8400
8405
8410
8415
8420
8425
8430
8435
8440
8445
8450
8455
8460
8465
8470
8475
8480
8485
8490
8495
8500
8505
8510
8515
8520
8525
8530
8535
8540
8545
8550
8555
8560
8565
8570
8575
8580
8585
8590
8595
8600
8605
8610
8615
8620
8625
8630
8635
8640
8645
8650
8655
8660
8665
8670
8675
8680
8685
8690
8695
8700
8705
8710
8715
8720
8725
8730
8735
8740
8745
8750
8755
8760
8765
8770
8775
8780
8785
8790
8795
8800
8805
8810
8815
8820
8825
8830
8835
8840
8845
8850
8855
8860
8865
8870
8875
8880
8885
8890
8895
8900
8905
8910
8915
8920
8925
8930
8935
8940
8945
8950
8955
8960
8965
8970
8975
8980
8985
8990
8995
9000
9005
9010
9015
9020
9025
9030
9035
9040
9045
9050
9055
9060
9065
9070
9075
9080
9085
9090
9095
9100
9105
9110
9115
9120
9125
9130
9135
9140
9145
9150
9155
9160
9165
9170
9175
9180
9185
9190
9195
9200
9205
9210
9215
9220
9225
9230
9235
9240
9245
9250
9255
9260
9265
9270
9275
9280
9285
9290
9295
9300
9305
9310
9315
9320
9325
9330
9335
9340
9345
9350
9355
9360
9365
9370
9375
9380
9385
9390
9395
9400
9405
9410
9415
9420
9425
9430
9435
9440
9445
9450
9455
9460
9465
9470
9475
9480
9485
9490
9495
9500
9505
9510
9515
9520
9525
9530
9535
9540
9545
9550
9555
9560
9565
9570
9575
9580
9585
9590
9595
9600
9605
9610
9615
9620
9625
9630
9635
9640
9645
9650
9655
9660
9665
9670
9675
9680
9685
9690
9695
9700
9705
9710
9715
9720
9725
9730
9735
9740
9745
9750
9755
9760
9765
9770
9775
9780
9785
9790
9795
9800
9805
9810
9815
9820
9825
9830
9835
9840
9845
9850
9855
9860
9865
9870
9875
9880
9885
9890
9895
9900
9905
9910
9915
9920
9925
9930
9935
9940
9945
9950
9955
9960
9965
9970
9975
9980
9985
9990
9995
10000
10005
10010
10015
10020
10025
10030
10035
10040
10045
10050
10055
10060
10065
10070
10075
10080
10085
10090
10095
10100
10105
10110
10115
10120
10125
10130
10135
10140
10145
10150
10155
10160
101

generally requires that the etch be performed with a hardmask. Furthermore, it is often desirable for part of the hardmask to remain on the ILD, to avoid a mask removal process which might damage the ILD; this layer is sometimes called a "residual
5 hardmask" or "permanent hardmask." Accordingly, the hardmask layer in contact with the low-k ILD should also have a low dielectric constant.

A typical hardmask for formation of lines and vias in the ILD is shown schematically in Figure 1A. The ILD 10 is
10 disposed on a barrier layer 1, which in turn covers the underlying level (not shown). The ILD is generally formed of a polymer such as an organic polyarylene ether thermoset dielectric, or a similar material. The hardmask includes three layers 11-13. Permanent hardmask layer 11 is formed of a low-k material ($k < 4.5$); examples of such materials are
15 organosilicates such as SiCOH (containing Si, C, O and H); SiC; SiC:H; and amorphous Si containing C and H. Layer 11 is covered by layer 12, typically silicon nitride; thicknesses of layers 11 and 12 are approximately 500 Å and 350 Å
20 respectively. Layer 13 is typically silicon dioxide with a thickness of approximately 1500 Å. The pattern for the metal lines is transferred to layer 13 ("line-level" lithography), resulting in formation of exposed areas 2 in the mask, as shown in Figure 1B. Further processing involves depositing a layer
25 of resist 14 which is patterned to define via openings 4 ("via-level" lithography), as shown in Figure 1C. This requires that the resist 14 be at least partially planarized over the topography introduced by patterning layer 13. Layer 13 is also subject to faceting (that is, formation of facets 3), which
30 leads to loss of critical-dimension control. The fidelity of the pattern transfer is also degraded by roughening of the line edge, caused by deposition thereon of plasma polymers.

Furthermore, as shown in Figure 1D, in subsequent processing the etched lines and via openings are overfilled

with metal 16 (often with a liner 15); the excess metal must then be removed, typically by chemical-mechanical polishing (CMP). If the metal 16 and liner material 15 are removed by CMP at nearly the same rate (for example, when metal 16 is copper and liner 15 is tungsten), the remaining hardmask must also function as a polish stop layer. The thin layer 12 of silicon nitride may not be effective as a CMP stop layer.

There is a need for an improved dual damascene process in which the hardmask structure permits processing with very high fidelity pattern transfer while retaining the advantages of low dielectric constant, and includes an effective CMP stopping layer.

SUMMARY OF THE INVENTION

The present invention addresses the above-described need by providing a dual damascene process using a hardmask structure including a sacrificial hardmask layer and which eliminates at least the oxide layer overlying the low-k dielectric layer.

In accordance with a first aspect of the invention, a method is provided in which three hardmask layers (lower, middle and top) are deposited on a low-k substrate. The top hardmask layer has a thickness less than about 200 Å. A first opening is formed in the top hardmask layer in accordance with a first pattern, thereby exposing a portion of the middle hardmask layer. A second opening is formed in that portion of the middle hardmask layer in accordance with a second pattern and a corresponding opening in the lower hardmask layer, thereby exposing a portion of the substrate. An opening is formed in the substrate, and metal is deposited therein. Excess metal may be deposited over the hardmask and then removed. Finally, the top hardmask layer is removed.

The material of the top hardmask layer may be a refractory

metal, a refractory metal nitride, a refractory metal alloy or a conductive Si-based material such as doped Si or doped amorphous Si, and is preferably a refractory metal nitride such as TaN. The middle hardmask layer is preferably SiN. The excess metal may be removed by CMP, with the top hardmask layer having a lower polishing rate than the excess metal being polished.

It should be noted that the process of forming the first opening may include depositing a resist layer on the top hardmask layer and subsequently removing the resist layer therefrom; the middle hardmask layer protects the lower hardmask layer from oxidation during removal of the resist layer.

In accordance with a second aspect of the invention, a method is provided in which a lower hardmask layer and a top hardmask layer are deposited. A protective layer is formed in a region of the lower hardmask layer adjacent to the top surface thereof; this protective layer protects the lower hardmask layer from oxidation when the resist removal is performed. The protective layer may be formed by exposing the lower hardmask layer to a plasma treatment which either forms a protective nitride layer in the top surface region, or densifies the lower hardmask layer in that region. The protective layer has a thickness of approximately 100 Å.

In accordance with an additional aspect of the invention, a method is provided in which a lower hardmask layer and a top hardmask layer are deposited on the substrate. A first opening is formed in the top hardmask layer in accordance with a first pattern, thereby exposing a portion of the lower hardmask layer. This process includes depositing a resist layer on the top hardmask layer and subsequently removing the resist layer therefrom; the resist layer is removed in a non-oxidizing resist strip process, so that oxidation of the lower hardmask layer is avoided. In particular, the resist may be removed in

a plasma resist strip process with a reducing chemistry.

It is noteworthy that the top hardmask layer is a thin sacrificial layer which can also serve as a CMP stopping layer, and that oxidation damage to the lower hardmask layer (which generally is of a low-k material) is avoided.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a schematic illustration of a typical hardmask structure used in dual damascene processing.

Figures 1B-1D illustrate some of the processing difficulties encountered using the hardmask of Figure 1A.

Figures 2A-2H illustrate a dual damascene process using a three-layer hardmask in accordance with a first embodiment of the invention.

Figures 3A-3H illustrate a dual damascene process using a two-layer hardmask in accordance with a second embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The hardmask structure of the present invention uses a thin (approximately 100-200 Å) sacrificial layer which overlies and protects the low-k dielectric hardmask layer, is an effective mask for etching the pattern of metal lines, and also provides an effective polishing stop in the metal CMP process.

First Embodiment: Three-layer hardmask

The structure of the hardmask of this embodiment is shown in Figure 2A. A thin hardmask layer 20 is used in place of the oxide layer 13 of the conventional hardmask (compare Figure 1A) and is the top layer of the three-layer hardmask structure. The underlying residual hardmask includes layer 11 and layer

12. The middle layer 12 is generally of a dielectric material having properties that are not degraded during typical processing steps (e.g. etching with a resist mask, resist strip, wet cleaning). This dielectric material may be SiO₂, SiN, SiON, SiOF, or a similar material known in the art. The bottom layer 11 is generally of a low-dielectric-constant material such as SiC, SiC:H, an organosilicate (e.g. SiCOH), SiCNH, a spin-on silsesquioxane, carbon-doped oxide, organosilicate glass, silicon oxycarbide, amorphous hydrogenated silicon carbide, amorphous hydrogenated silicon carbide/nitride, or a similar suitable material. It will be appreciated that this layer is subject to damage in various typical processing steps, and therefore requires a protective layer (in this case, dielectric layer 12). In particular, the low-k layer 11 must be protected from oxidation during deposition of layer 20 and during resist strip processes (e.g. during resist rework).

Layer 20 may be a metal, metal compound or alloy, semiconductor or dielectric, provided at least that (i) the deposition of layer 20 does not damage the underlying layers, and in particular does not alter the desirable electrical properties of layers 10 and 11; and (ii) the polishing rate of layer 20 is low compared to that of the excess metal removed by CMP. Layer 20 is preferably a refractory metal (e.g. Ta, Ti, W), a refractory metal nitride (e.g. TaN, TiN, WN), a refractory metal alloy (e.g. TaSiN, TiSiN, WSiN, TiW), a conductive Si-based material such as doped Si or doped amorphous Si, or some other metal (e.g. Cu, Al, Ag). More preferably, layer 20 is formed of a refractory metal nitride. In particular, it has been found that a 150 Å layer of TaN provides good pattern fidelity while maintaining the desirable properties of layers 10 and 11.

In this embodiment, the ILD layer 10 is formed of an organic polyarylene ether thermoset dielectric; the residual

hardmask layers 11 and 12 are SiC and SiN respectively; and layer 20 is formed of TaN. Layers 11 and 12 may be formed by chemical vapor deposition (CVD) or plasma enhanced CVD. Layer 11 may also be deposited in a spin-on process. Layer 20 may be formed by physical vapor deposition or CVD.

Figures 2B-2H illustrate steps in a dual damascene process using the hardmask of this embodiment. A resist layer 21 is applied over the hardmask, and the pattern of metal lines is developed therein. The line-level pattern is transferred to the mask by etching openings 22 in layer 20, using Cl_2 or Cl_2/BCl_3 chemistry (Figure 2B). The resist layer 21 is then stripped and resist residues are removed, using methods known in the art. Another resist layer 23 is then applied over the mask, and the pattern of via openings 24 is developed therein (Figure 2C). Compared to oxide layer 13, layer 20 is much less subject to faceting and introduces much less topography (compare Figures 1C and 2C).

The dual-damascene pattern is transferred first to the residual hardmask, and then to the ILD, in a sequence of etching steps. Layers 11 and 12 are etched using a fluorocarbon-based chemistry. The ILD layer 10 is then partially etched using a chemistry including one or more of O_2 , O_3 , SO_2 , SO_3 , N_2 , NH_3 , N_2H_2 , N_2H_4 , H_2 , CO_2 , CO , CF_4 , CHF_3 , CH_2F_2 or CH_3F ; during this etch the resist layer 23 is also removed (Figure 2D). An additional fluorocarbon-based etch is then performed with layer 20 as a mask, opening layers 11 and 12 of the hardmask in accordance with the metal line pattern (openings 22). A further etching step, using chemistry similar to that of the previous partial via etch, transfers the line-level pattern into the ILD and completes the formation of the vias (openings 24). As shown in Figure 2E, the metal line pattern is transferred into the upper portion of the substrate and the via pattern is transferred into the lower portion of the substrate. This etching step stops at barrier layer 1,

which typically is formed of SiN or SiC. A fluorocarbon-based etch then is used to open the barrier layer, so that metallization of the via may contact the underlying level 100. The width of the opening 24 at the bottom of the via may be as small as approximately 100 nm.

The metallization process preferably involves deposition of a liner 25, followed by deposition of metal 26 in the vias, in the metal line pattern, and over the hardmask (Figure 2F). The excess metal is then polished away using a CMP process; the portion of the liner 25 overlying the hardmask layer 20 is generally also removed in the same CMP process. In particular, if liner 25 is W while metal 26 is Cu, a standard CMP process will not be selective between the two. It is necessary in such a case for layer 20 to serve as a polishing stop (Figure 2G). A typical CMP process for Cu will not be stopped by W but will be stopped by Ti, Ta, TiN or TaN. Accordingly, a layer of TaN, as described in this embodiment, provides an effective polishing stop. Layer 20 is then removed in a separate polishing process. At this point it is desirable to remove layer 12 also, so that only the low-k layer 11 of the hardmask structure remains (Figure 2H).

The hardmask structure of this embodiment provides greatly improved control of the critical dimension (metal line width and spacing) compared to the hardmask structure of Figure 1A. In addition, the hardmask of the present embodiment provides an effective polishing stop, which in turn permits development of a more reliable CMP metal removal process.

Second Embodiment: Two-layer hardmask

The structure of the hardmask of this embodiment is shown in Figure 3A. Repeated reference numerals between Figures 2A-2H and 3A-3H indicate corresponding structures. As in the first embodiment, a thin sacrificial hardmask layer 20 comprises the top layer of the hardmask. The material of layer

20 may be a refractory metal (e.g. Ta, Ti, W), a refractory metal nitride (e.g. TaN, TiN, WN), a refractory metal alloy (e.g. TaSiN, TiSiN, WSiN, TiW), a conductive Si-based material such as doped Si or doped amorphous Si, or some other metal (e.g. Cu, Al, Ag). A preferred material is TaN, with a thickness of about 150 Å. The underlying layer 31 is a low-k dielectric such as SiCOH or a similar material as in layer 11 of the first embodiment, with a thickness of about 500 Å.

In the present embodiment, the intermediate hardmask layer (such as nitride layer 12) is eliminated; compare Figures 2A and 3A. This is done by (i) treating the low-k layer 31 to make it resistant to processing damage (e.g. damage by oxidation during a resist strip process) and/or (ii) using a resist strip process which does not oxidize the exposed surface of layer 31.

Layer 31 may be deposited on the ILD layer 10 using CVD or plasma-enhanced CVD. In this embodiment, a 500 Å thickness of SiCOH is deposited by plasma-enhanced CVD. The surface of layer 31 is then exposed to a plasma (e.g. an NH₃ or nitride-based plasma) which causes formation of a nitride in the top surface region 31t of layer 31. Alternatively, the surface of layer 31 may be exposed to a plasma treatment which densifies the layer in surface region 31t, or layer 31 may be deposited under conditions such that the material has increased density in region 31t. The top surface region 31t has a thickness of about 100 Å.

In another alternative, the need for plasma treatment or densification of the low-k layer 31 may be avoided by using resist strip processes which do not oxidize the surface of layer 31, as discussed in more detail below.

The top hardmask layer 20 is then deposited on layer 31; in this embodiment, a 150 Å thickness of TaN is deposited by physical vapor deposition (PVD). As noted above, layer 20 may be a metal, semiconductor or dielectric, provided that the

deposition process for layer 20 does not alter the properties of layer 31, and that the polishing rate of layer 20 is low compared to that of the metal used for the conducting lines.

Figures 3B-3H illustrate steps in a dual damascene process using the two-layer hardmask of this embodiment. A resist layer 21 is applied over the hardmask; line-level patterning is then performed wherein hardmask layer 20 is patterned to produce openings 22 in accordance with the pattern of metal lines, using Cl_2 or Cl_2/BCl_3 chemistry (Figure 3B).

The resist layer 21 is then stripped using a non-oxidizing, reducing, or mildly oxidizing plasma process. This process is preferably a plasma process with a reducing chemistry; most preferably, an NH_3/H_2 or N_2/H_2 plasma process which prevents oxidation of the exposed surface of layer 31. Alternatively, a selective solvent-based resist strip process may be used, such as an acetone-based acidic resist strip.

The via-level patterning is then performed, wherein resist layer 23 is applied and the pattern of via openings 24 is developed therein (Figure 3C). As in the first embodiment, the line level pattern and via level pattern are transferred to the hardmask layer 31 and the ILD layer 10. The via pattern is etched into the SiCOH layer 31. A partial via etch is then performed, in which the via pattern is transferred into the ILD layer 10 (Figure 3D). The resist layer 23 is also removed during this partial via etch step. An additional etch is then performed with layer 20 as a mask, opening layer 31 in accordance with the metal line pattern (thus creating openings 22 in the mask layer 31). A further etching step, using chemistry similar to that of the previous partial via etch, transfers the line-level pattern into the upper portion of the ILD and completes the formation of the vias through the lower portion of the ILD (openings 24), as shown in Figure 3E.

The metallization process (preferably including deposition of liner 25 and metal 26) is then performed, resulting in the

structure shown in Figure 3F. The excess metal and exposed liner are then polished away using a CMP process, with layer 20 serving as a polishing stop layer as in the first embodiment. After the excess metal is polished (Figure 3G), layer 20 is removed in a separate polishing process to yield the structure shown in Figure 3H. It may be desirable to also remove the surface region 31t of layer 31 by CMP.

It is noteworthy that in this embodiment, the entire residual hardmask (consisting of layer 31) is a low-k material, along with the ILD layer 10.

The hardmask of the present embodiment offers all the advantages of the first embodiment, and in addition permits reduced process complexity and faster processing time, owing to the elimination of one layer from the conventional hardmask structure.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.